WHAT IS CLAIMED IS:

1. A clock synthesizer apparatus, comprising:

a clock and data recovery (CDR) circuit including a serial data input, said CDR circuit operable when a serial data stream is applied thereto via said serial data input for recovering a clock signal from the serial data stream;

a clock source input for receiving a clock source signal having a fixed transition density, said clock source input coupled to said serial data input for applying said clock source signal to said CDR circuit; and

said CDR circuit responsive to said clock source signal received at said serial data input thereof for producing a desired clock signal.

2. The apparatus of Claim 1, wherein said CDR circuit has a loop bandwidth between 100 KHz and 1.5 MHz.

3. The apparatus of Claim 1, wherein said CDR circuit has a loop bandwidth of approximately 1 MHz.

4. The apparatus of Claim 1, wherein said CDR circuit has a programmable loop bandwidth.

5. The apparatus of Claim 1, wherein said desired clock signal is a serialization clock signal for use in converting parallel data into a serial data stream.

6. The apparatus of Claim 1, wherein said CDR circuit includes a first node where the recovered clock signal is provided when a serial data stream is applied to said serial data input, and said CDR circuit having a second node where said desired clock signal is provided when said clock source signal is applied to said serial data input, and wherein said first and second nodes are electrically distinct from one another.

7. The apparatus of Claim 1, including a divide-by-two circuit connected between said clock source input and said serial data input.

8. A serial data transceiver apparatus, comprising:

a receive data input for receiving an input serial data stream;

a first clock and data recovery (CDR) circuit coupled to said receive data input for deserializing said input serial data stream;

a data serializer for converting parallel data into an output serial data stream, said data serializer having a clock input for receiving a transmit serialization clock signal, said data serializer for producing said output serial data stream based on said transmit serialization clock signal;

a clock synthesizer apparatus coupled to said clock input for providing said transmit serialization clock signal, including a second CDR circuit having a serial data

input, said second CDR circuit operable when a serial data stream is applied thereto via said serial data input for recovering a clock signal from the serial data stream, said clock synthesizer apparatus including a clock source input for receiving a clock source signal, said clock source input coupled to said serial data input for applying said clock source signal to said second CDR circuit, said second CDR circuit responsive to said clock source signal for producing said transmit serialization clock signal; and

a transmit data output coupled to said data serializer for transmitting said output serial data stream.

9. The apparatus of Claim 8, provided as a SONET transceiver.

10. The apparatus of Claim 8, provided as an SFI-5 transceiver.

11. The apparatus of Claim 8, provided as a FiberChannel transceiver.

12. The apparatus of Claim 8, provided as a Xaui transceiver.

13. The apparatus of Claim 8, including a selector having an output coupled to said serial data input, wherein said first CDR circuit is for recovering a clock signal from said input serial data stream, said selector having a first input coupled to said clock source input for receiving said clock source signal, and having a second input coupled to said first CDR circuit for receiving said recovered clock signal.

14. The apparatus of Claim 13, wherein each of said CDR circuits has a PLL clock input for receiving first and second PLL clocks, and including a PLL having an output for providing said first and second PLL clocks, each of said CDR circuits having said PLL clock input thereof coupled to said PLL output for receiving said first and second PLL clocks.

15. The apparatus of Claim 14, wherein each of said first and second CDR circuits attenuates low frequency phase noise components of said first and second PLL clocks.

16. The apparatus of Claim 8, wherein said second CDR circuit has a loop bandwidth that is lower than a loop bandwidth of said first CDR circuit.

17. The apparatus of Claim 8, wherein each of said CDR circuits has a PLL clock input for receiving first and second PLL clocks, and including a PLL having an output for providing said first and second PLL clocks, each of said CDR circuits having said PLL clock input thereof coupled to said PLL output for receiving said first and second PLL clocks.

18. The apparatus of Claim 17, wherein each of said first and second CDR circuits attenuates low frequency phase noise components of said first and second PLL clocks.

19. The apparatus of Claim 18, wherein said second CDR circuit rejects high frequency noise components said clock source signal.

20. The apparatus of Claim 8, wherein said second CDR circuit low-pass filters said clock source signal.

21. The apparatus of Claim 20, including a selector having an output coupled to said serial data input, wherein said first CDR circuit is for recovering a clock signal from said input serial data stream, said selector having a first input coupled to said clock source input for receiving said clock source signal, and having a second input coupled to said first CDR circuit for receiving said recovered clock signal.

22. A method of synthesizing a clock signal, comprising:

providing a clock source signal having a fixed transition density; and

performing on said clock source signal a clock and data recovery (CDR) operation which produces a desired clock signal in response to said clock source signal.

23. The method of Claim 22, wherein the desired clock signal is a serialization clock signal for use in converting parallel data into a serial data stream.

24. The method of Claim 22, wherein said performing step includes filtering said clock source signal in the digital domain.

25. A serial data transceiver apparatus, comprising:

means for deserializing an input serial data stream;

means for converting parallel data into an output serial data stream based on a transmit serialization clock signal; and

means for producing said transmit serialization clock signal by applying a CDR operation to a clock source signal.

26. A serial data transceiver apparatus, comprising:

a receive data input for receiving an input serial data stream;

a clock and data recovery (CDR) circuit coupled to said receive data input for recovering a receive clock signal from said input serial data stream;

a data serializer for converting parallel data into an output serial data stream, said data serializer having a clock input for receiving a transmit serialization clock signal, said data serializer for producing said output serial data stream based on said transmit serialization clock signal;

a clock synthesizer apparatus coupled to said clock input for providing said transmit serialization clock signal;

said CDR circuit and said clock synthesizer apparatus having respective PLL clock inputs, each said PLL clock input for receiving first and second PLL clocks; and

a PLL having an output for providing said first and second PLL clocks, said CDR circuit and said clock synthesizer apparatus each having said PLL clock input thereof coupled to said PLL output for receiving said first and second PLL clocks.

27. A serial data transceiver apparatus, comprising:

means for recovering a received clock signal from an input serial data stream based on first and second PLL clocks;

means for producing a transmit serialization clock signal based on said first and second PLL clocks; and

means for converting parallel data into an output serial data stream based on said transmit serialization clock signal.

28. A method of transmitting and receiving serial data, comprising:

recovering a receive clock signal from an input serial data stream based on first and second PLL clocks;

producing a transmit serialization clock signal based on said first and second PLL clocks; and

converting parallel data into an output serial data stream based on the transmit serialization clock signal.